

REMARKS

As an initial matter, Applicants appreciate the Examiner's acknowledgement that claims 2-7, 9-14, and 16-21 contain allowable subject matter. Claims 8 and 9 have been amended. Claims 1-21 remain pending. For the reasons that follow, reconsideration and withdrawal of all outstanding rejections and objections are requested.

Claims 22-23 remain withdrawn. The Office Action maintains the previous restriction requirement of these claims, stating that searching the method "of forming a semiconductor device requires a different thought process and class in searching than the semiconductor device structure." Office Action, at 2. Claim 23, however, relates to a semiconductor device, not a method of formation. For at least this reason, Applicants respectfully request that the Examiner reconsider this restriction, at least with respect to claim 23.

Claims 1, 8 and 15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,386,135 to Nakazato et al. ("Nakazato") in view of U.S. Patent No. 5,913,114 to Lee et al ("Lee"). The rejection is traversed, and reconsideration is requested.

The present invention relates to a semiconductor device including both DMOS and CMOS transistors on a single substrate. Claims 1 and 15 each require a p-channel DMOS transistor and a CMOS transistor disposed on one p-type substrate. Independent claim 8 has been amended to recite an n-channel DMOS and a CMOS transistor on one common n-type substrate comprising "a first N-type low concentration region over an N-type high concentration substrate region." Neither reference, whether considered alone or in combination, teaches the unique combination of limitations recited by claims 1, 8, and 15.

Nakazato, for example, provides no teaching or suggestion of the claimed "DMOS transistor" as recited by any of claims 1, 8, or 15. The Office Action relies on the pMOS transistor "pMOS3" in Nakazato's FIG. 33 as teaching the DMOS transistor, but this is inaccurate. pMOS3 is the p-channel transistor complement to nMOS3, to form a CMOS structure. pMOS3 does not relate to a DMOS transistor, and in fact, Nakazato provides no teaching whatsoever with respect to DMOS transistors.

Nor does Lee cure the deficiencies of Nakazato. Specifically, with reference to claims 1 and 15, Lee provides no teaching of a "p-channel DMOS transistor disposed on the p-type semiconductor substrate" as recited by these claims. Rather, Lee teaches only an n-channel DMOS transistor being formed in an n-type substrate 300 (see Fig. 14 and accompanying text). With respect to claim 8, Lee provides no teaching of an n-type substrate comprising "a first N-type low concentration region over an N-type high concentration substrate region." In contrast, Lee teaches providing a substrate comprising a n-type region 300 formed over a p-type main substrate portion 10.

For at least these reasons, Applicants submit that independent claims 1, 8, and 15 are allowable, as well as claims 2-7, 9-14, and 16-21, for which the allowability has been acknowledged. Based on the foregoing, applicants believe the application, including at least claims 1-21 and 23, is in condition for immediate allowance.

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